UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/791,256 | 03/02/2004 | John J. Sidorowich | TWI-11120 | 2789 |

28584 7590 11/10/2005

STALLMAN & POLLOCK LLP
SUITE 2200
353 SACRAMENTO STREET
SAN FRANCISCO, CA 94111

| EXAMINER | |
|---|---|
| NGUYEN, SANG H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2877 | |

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/791,256 | SIDOROWICH, JOHN J. | |
| | Examiner | Art Unit | |
| | Sang Nguyen | 2877 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *38-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This application is a Continuation of application serial number 10/349,262 filed on 01/22/03 issued Patent No. 6,781,706 that is a Continuation of 09/542,724 filed on 04/04/00 issued Patent No. 6,532,076.

### *Response to Pre-Amendment*

Pre-Amendment filed on 03/02/04 has been entered. It is noted that the application contains claims 38-42 and claims 1-37 have been canceled by the Pre-Amendment on 03/02/04.

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on 03/02/04 has been entered. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, Others Documents and US Patents of the information disclosure statement provided in application serial number 10/349,262 filed on 01/22/03 issued Patent No. 6,781,706 that is being considered by the examiner.

### *Oath/Declaration*

The oath/declaration filed on 03/02/04 is acceptable.

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

**Claims 38-42 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of U.S. Patent No. 6,781,706 in view of Gold et al (U.S. Patent No. 4,999,014).**

**Regarding claim 38**; all of features of claims 1-5 of U.S. Patent No. 6,781,706 discloses a multidomain process of a system for evaluating parameters of a semiconductor wafer or wafer set (claim 1 lines 1-2 and col.9 lines 44-45), comprising:

generate measurement data, based on the received signals, for multiple points on the semiconductor wafer or wafer set (claim 1 in lines 3-4 and col.9 lines 46-47), and to define multiple domains, wherein a domain has corresponding measured data (claim 1 lines 5-6 and col. 9 lines 48-49) , and to determine an optimum group of parameter values for each domain, wherein to determine the optimum group for each domain with an iterative search method (claim 1 lines 7-10 and col.9 lines 50-53) including:

associate different sets of theoretical semiconductor wafer parameter values with each domain (claim 1 lines 15-16),

compare a first set of theoretical measurement data, derived from a first set of theoretical semiconductor wafer parameter values associated with a domain, to the measured data corresponding to the domain (claim 1 lines 17-20), and

generate a new set of theoretical semiconductor wafer parameter values to be associated with the domain based on the comparing in a manner so as to associate increasingly more optimal theoretical semiconductor wafer parameter values with the domain, wherein the generation of the new set of theoretical semiconductor parameter values includes migrating at least one theoretical semiconductor parameter value from a set of theoretical semiconductor parameter values that has been associated with a different domain (claim 1 lines 21-31).

Claims 1-5 of U.S. Patent No. 6,781,706 teaches all of features of claimed invention as indicate above except for a system having a source which generates a probe beam which is transmitted through a lens and onto a semiconductor wafer, a detector which detects the probe beam after it is reflected off the semiconductor wafer, and the detector outputs signals based on the probe beam reflected of the semiconductor wafer. However, Gold et al teaches that it is known in the art to provide a system (20 of figure 1) having a light source (22 of figure 1) which generates a probe beam (24 of figure 1) which is transmitted through a lens (30 of figure 1) and onto a semiconductor wafer considered to a thin film (32 of figure 1) deposited on a sample substrate (28 of figure 1), a detector (50 of figure 1) which detects the probe beam (24 of figure 1) after it is reflected off the semiconductor wafer (32,28 of figure 1), the detector (50 of figure 1) outputs signals based on the probe beam reflected of the semiconductor wafer (32, 28 of figure 1), and a processor (52 of figure 1) coupled to the detector (50 of figure 1) to receive the signals. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine Claims 1-5

of U.S. Patent No. 6,781,706 with a system having a source which generates a probe beam which is transmitted through a lens and onto a semiconductor wafer, a detector which detects the probe beam after it is reflected off the semiconductor wafer, and the detector outputs signals based on the probe beam reflected of the semiconductor wafer as taught by Gold et al for the purpose of measuring accuracy of parameters (as thickness) of the semiconductor measurement can be further enhanced by measuring the full power of the reflected probe beam (col.11 lines 40-43).

**Regarding claim 39**; all of features of claim 2 of U.S. Patent No. 6,781,706 discloses the processor is programmed such that the new set of theoretical semiconductor wafer parameter values are generated in accordance with a genetic algorithm (claim 2 lines 1-4 and col. 10 lines 8-11).

**Regarding claim 40**; all of features of claims 1 and 3 of U.S. Patent No. 6,781,706 discloses the processor is programmed such that the processor generates a plurality of sets of theoretical semiconductor wafer parameter values, and wherein the generating a plurality of sets of theoretical wafer parameter values includes defining a plurality of genotypes wherein a genotype includes a plurality of genes, wherein the plurality of genes correspond to different wafer parameters (claim 3 lines 1-5), and derives a set of theoretical measurement data for each set of theoretical semiconductor wafer parameter values (claim 1 lines 12-14).

**Regarding claim 41**; all of features of claim 4 of U.S. Patent No. 6,781,706 discloses the processor is programmed such that one or more of the plurality of genes is defined as belonging to a first class where genes of the first class are optimized for

each domain, and one or more of the plurality of genes is defined as belonging to a second class where genes of the second class are optimized across a plurality of domains, and one or more of the plurality genes is defined as belonging to a third class where genes of the third class are optimized across all domains, such that the genes of the third class are deemed to have the same value for each domain (claim 4 lines 1-10).

**Regarding claim 42**; all of features of claim 4 of U.S. Patent No. 6,781,706 discloses the processor is programmed such that each of the genes of the plurality of genes is defined as belonging to one class of a group of different gene classes, wherein the group of different gene classes includes a first class where genes of the first class are optimized for each domain, a second class where genes of the second class are optimized across a plurality of domains, and a third class where genes of the third class are optimized across all domains, such that the genes of the third class are deemed to have the same value for each domain (claim 5 lines 1-10 and col. 10 lines 28-38).

***Allowable Subject Matter***

**Claims 38-42 would be allowable if applicant filed a terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b) to overcome the rejection(s) under the judicially created doctrine of obviousness-type double patenting, set forth in this Office action.**

As to independent claim 38 is allowable over the prior art for at least the reason that the prior art of record, taken alone or in combination, fails discloses or render obvious a system for evaluating parameters of a semiconductor wafer comprising all the specific elements with the specific combination including of determine an optimum

group of parameter values for each domain, wherein to determine the optimum group for each domain the processor is operable to: associate different sets of theoretical semiconductor wafer parameter values with each domain, compare a first set of theoretical measurement data, derived from a first set of theoretical semiconductor wafer parameter values associated with a domain, to the measured data corresponding to the domain, and generate a new set of theoretical semiconductor wafer parameter values to be associated with the domain based on the comparing in a manner so ms 'to associate increasingly more optimal theoretical semiconductor wafer parameter values with the domain, wherein the generation of the new set of theoretical semiconductor parameter values includes migrating at least one theoretical semiconductor parameter value from a set of theoretical semiconductor parameter values that has been associated with a different domain in combination with the rest of the limitation of claim 38.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al (6268916) discloses system for non-destructive measurement of samples; Willenborg et al (5159412) teaches optical measurement device with enhanced sensitivity; or Carver (4652757) discloses method and apparatus for optically determining defects in a semiconductor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sang Nguyen whose telephone number is (571) 272-2425. The examiner can normally be reached on 9:30 am to 7:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory J. Toatley, Jr. can be reached on (571) 272-2800 ext. 77. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 8, 2005

**Patent Examiner**
**Sang Nguyen**
**Art Unit 2877**